An Overview of High Speed Implementation of 16 x 16 Multiplier Using Vedic Mathematics

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Abstract – Vedic arithmetic is that the traditional system of arithmetic which has a novel technique of calculations supported sixteen Sutras that are discovered by Sri Bharti Krishna Tirthaji. Any processor’s performance depends on 3 vital factors specifically speed, space and power. A higher trade-off between these factors makes the processor, a good one. Multipliers are the usually used architectures within the processor. If the performance of those multipliers is improved then powerful processors is created in future. During this paper, the planned number style supported the sutra ‘Urdhva Tiryakbhyam’ of Vedic arithmetic is analyzed and also the performance results of the number are compared with standard multipliers. Extremely economical arithmetic operations are necessary to appreciate the specified performance in several period of time systems and digital image method applications. Altogether these applications, one of the necessary arithmetic operations of performed is to multiply and accumulate with a little method time (delay).

Keywords: Vedic multiplier, Array Multiplier, Vedic Mathematics, Urdhva-Tiryagbhyam.

I. Introduction

A N X N bit parallel overlay multiplier factor design is intended for top speed DSP operations. The design relies on the vertical and crosswise algorithmic rule of ancient Indian Vedic arithmetic. so the performance of the multiplier factor may be a key component in crucial the presentation of the complete system. this can be because; the multiplier factor is that the slowest and most time intense consider the system. so the optimisation of the multiplier factor speed and space may be a most significant challenge for the structure designers. In his challenge is also successfully overcome by the utilization of ancient Vedic arithmetic. Vedic arithmetic is one of the foremost ancient methodologies used by the Aryans therefore on perform mathematical computation [2]. It consists of algorithm rule that ought to boil down large arithmetic operations to simple mind calculations. The efforts place by Jagadguru swami Sri Bharti avatar Tirtha maharajah to introduce Vedic arithmetic to the commoners additionally as contour Vedic Algorithms into Sixteen classes [1] or Sutras must be acknowledged and appreciated. Sri Bharti Krishna Tirthaji (1884-1960) planned the idea of Vedic arithmetic when his eight years of analysis on Atharva Vedas [1]. This branch of arithmetic depends on sixteen Sanskrit literature. Vedic arithmetic may be a terribly fascinating field and presents some effective algorithms which will be applied to a range of division of engineering like estimate and digital signal processing. Associating multiplication with Vedic arithmetic methodology would lead to the buildup of procedure time.

The multiplier factor design relies on the Vertical and Crosswise algorithmic rule of antique Indian Vedic arithmetic. several Digital signal processing (DSP) systems includes multipliers jointly of core hardware blocks. Multipliers hold a major role in numerous DSP applications like digital filtering; electronic communication and fast Fourier transform [4]. The common classification of multipliers betting on their design involves 3 types: ‘serial multipliers’, ‘parallel multipliers’ and ‘serial-parallel multipliers’. during this paper, multiplier factor design supported Urdhva...
tiryakbhyam Sanskrit literature [6], a concept supported Vedic arithmetic is mentioned. Proposed paper uses Vedic-mathematics based mostly approach to cut back the quantity of partial merchandise for multiplication, that in-effect reduces the quantity of adders. Vedic arithmetic is that the ancient Indian system of arithmetic that relies on sixteen sutras and its sub-sutras mentioned in Atharva-Veda, and deals with numerous branch of arithmetic like arithmetic, algebra, geometry, trigonics, astronomy, calculus etc.

II. Literature Survey

Jagadguru Swami Sri Bharti Krishna Tirthaji Maharaja [1] “Vedic arithmetic or Sixteen easy Mathematice Formulae from the Veda”, the utilization of Vedic arithmetic lies within the undeniable fact that it reduces normal quality calculation within the standard arithmetic to terribly simple once, this will be so as a result of the Vedic formulae have claimed to be building on the natural principles on that the human mind works. Vedic arithmetic is also a many effective algorithms, that has cowl to various branches of engineering like computing. during this work, I even have studied fully completely different multipliers, which offer low power demand and high speed, jointly offer information of “urdhva-Tiryagbhyam” algorithmic rule of ancient Indian Vedic arithmetic, that has used for multiplication to reinforce speed, space parameters of multipliers.

Sudeep. M. C, Sharath Bimba. M, Mahendra Vucha [2] “Design and FPGA Implementation of High Speed Vedic Multiplier”, Multiplication is an operation abundant required in Digital Signal method for numerous applications. This paper puts forward a high speed Vedic multiplier that is economical in terms of speed, making use of Urdhva Tiryagbhyam, a Sanskrit literature from Vedic maths for multiplication and Kogge Stone algorithm for humanities addition of partial product and in addition compares it with the characteristics of existing many algorithms.

G.Vaithiyanathan, K.Venkatesan, S.Siva, S. Jayakumar, and S.Sivaramakrishnan, [3] “Simulation and Implementation of Vedic multiplier factor exploitation VHDL Code” during a typical processor, Multiplication is one in every of the essential arithmetic operations and it wants well a great deal of hardware resources and quantity than addition and subtraction. In detail, 8.72% of all the instruction in typical method units is multipliers. In computers, a typical central process unit devotes a substantial quantity of your time interval in implementing arithmetic operations, considerably multiplication operations.

G.Ganesh Kumar, V.Charishma [4] “Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques” it provides the planning of high speed Vedic number exploitation the techniques of Ancient Indian Vedic arithmetic that are customised to induce higher performance. Vedic arithmetic is that the ancient system of arithmetic that includes a distinctive technique of calculations supported sixteen Sutras.

Manoranjan Pradhan, et. al [5] “Speed Comparison of 16x16 Vedic Multipliers”, in this paper provides the extends multiplication to 16x16 Vedic multiplier factor exploitation “Nikhilam Sutra” technique. The 16x16 Vedic multiplier factor half victimization Urdhva Tiryagbhyam Sanskrit literature uses four 8x8 Vedic multiplier factor modules; one 16 bit carry save adders, and two 17 bit full adder stages. The carry save adder within the multiplier factor design will increase the speed of addition of partial product.

III. Method

III.1. Vedic Mathematics

The multiplier factor is predicated on an algorithmic rule Urdhva Tiryakbhyam (Vertical and Crosswise) of ancient Indian Vedic arithmetic. Urdhva Tiryakbhyam Sanskrit literature is general multiplication formula applicable to any or all case of multiplication. it's supported a unique idea through that generation of all partial product is done them; simultaneous addition of those partial product is done. therefore similarity in generation of partial product is obtained by exploitation Urdhva Tiryakbhyam Sanskrit literature. The summation of the parallel product is completed by employing a high power carry save adder. The partial product and their sums are calculative in parallel blocks, therefore the multiplier factor path delay won't contribute to the important path delay of the system. The principles of Vedic arithmetic is directly enforced in issues relating to pure mathematics functions, differential and the calculus, plane and sphere pure mathematics,
conics and completely different methods of applied math.

III.2. Vedic Multiplier

For implementation of 16 x 16 multiplier factor during this paper use 2 x 2 Vedic number because the basic building block. Here, “Urdhva-Tiryagbyham Sutra” or “Vertically and Crosswise Algorithm” for multiplication has been effectively wont to develop digital multiplier factor design. This technique explains {the a pair of[the 2} x 2 Vedic number module is enforced exploitation four 2-input AND gates and two half-adders. This algorithmic rule is completely different from the normal algorithmic rule like array multiplier factor that is employed to feature and shift the partial product the 2, 2-bit range multiplication.

III.3. Array Multiplier

In Array multiplier factor, AND gates are used for generation of the bit-products and adders for accumulation of generated bit product. All bit-products are generated in parallel and picked up through an array of full adders or the other kind of adders. Since the array multiplier factor has an everyday structure, wiring and also the layout are tired a far simplified manner. Therefore, among different multiplier factor structures, array multiplier factor takes up the smallest {amount} amount of space. however it's additionally the slowest with the latency proportional to O (Wct), wherever Wd is that the word length of the quantity.

Example 1:

![Example1 for Array multiplier 4X4](image)

In this paper, proposed High Speed Implementation of 16 x 16 multiplier factor exploitation Vedic arithmetic. Vedic multiplier factor is economical than Array multiplier factor. because the range of bit will increase from 8 x 8 bit to 16 x 16 bit, the temporal order delay greatly reduces for Vedic multiplier factor as compared to array multiplier factor, therefore the planned multiplier factor provides higher performance for higher order bit multiplication. within the planned multiplier factor for higher order bit multiplication i.e. for 16x16 and a lot of, the multiplier factor is accomplished by instantiating the lower order bit multipliers like 8x8. this can be primarily because of memory constraints. because of factors of temporal order potency, speed, lesser space, the planned Vedic parallel overlay design is enforced in Arithmetic and Logical Units substitution the normal number design. the planning is technology freelance and might be simply born-again from one technology to a different. additionally because of their Vertical and Crosswise structure the planning layout is easy and regular.

References


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